An Efficient Communication Protocol for Single- and Multi-Module Isolated Digital Power Supplies Using a Single Pulse-Transformer

Zhiyuan Hu[1]
Student Member, IEEE
zhiyuan.hu@Queensu.ca

Yan-Fei Liu[1]
Senior Member, IEEE
yanfei.liu@Queensu.ca

Tet Hin Yeap[2]
Member, IEEE
tet@site.uOttawa.ca

[1] Department of Electrical and Computer Engineering, Queen's University, Kingston, Ontario, K7L 3N6, Canada
[2] School of Information Technology and Engineering, University of Ottawa, Ottawa, Ontario, K1N 6N5, Canada

Abstract – **In this paper, an 8B/10B-based protocol is developed to optimize communications for single- and multi-module isolated digital power supplies. The protocol allows multiplexed feedback communications which transmits the feedback data of multiple power stages using a single pulse-transformer, which saves substantial cost of high-speed isolators. The protocol consumes less bandwidth than existing protocols. Experimental results of a prototype demonstrate the feasibility of the proposed system.**

Index Terms – **Feedback communication, Communication protocols**

I. INTRODUCTION

Digital power supplies promise improved performance by applying advanced digital control techniques such as digital proportional-integral-derivative (PID) control [1][2][3], fuzzy logic control [4][5], and other novel non-linear control strategies [6][7][8] into power supply systems. It reduces the amount of external components and increases the system flexibility [9][10]. However digital power looks promising, it must bring down the cost in order to enter the market.

Many electric applications contain multiple isolated power supply modules, such as Plasma TVs, LCD TVs, medical equipment, bench top power supplies, and so on. While going digital, each power module uses several high-speed isolators to transmit sample data and control functions such as On/Off, Over Voltage/Load/Temperature Protection, etc., as shown in Fig. 1 (a). Commonly used logic opto-couplers and pulse-transformers have a bandwidth of tens of mega bits per second. A few opto-couplers (e.g. Agilent HCPL901J) and RF-coupler isolators (e.g. Silicon Laboratories SI8442-C-IS) can achieve over 100Mbps but they are fairly expensive. The latest researches extended this record to 200 MHz [11][12][13].These high-speed isolators will quickly add up the cost to more than make sense.

An architecture that integrates all digital signals into one data bus can save substantial cost of the high-speed isolators, as shown in Fig. 1 (b). The sampling block samples the output voltage of each power stage. The encoder encodes the sample data and control commands, and transmits to the primary side through a shared communication bus. Only one isolator is used, and a phase-lock loop (PLL) is used on the primary side to recover the clock. The decoder decodes the data and uses them for control-law calculation and other functions.

(a) Traditional digital power supply systems
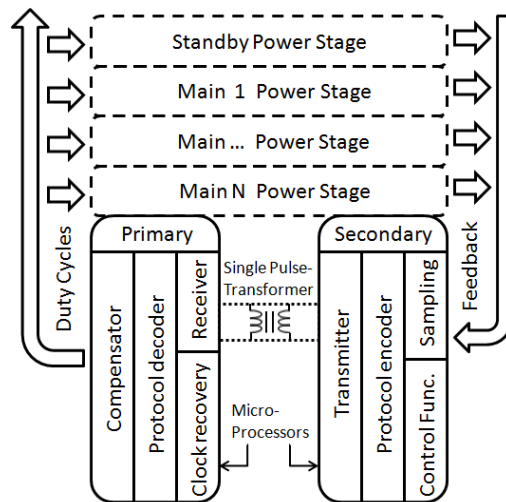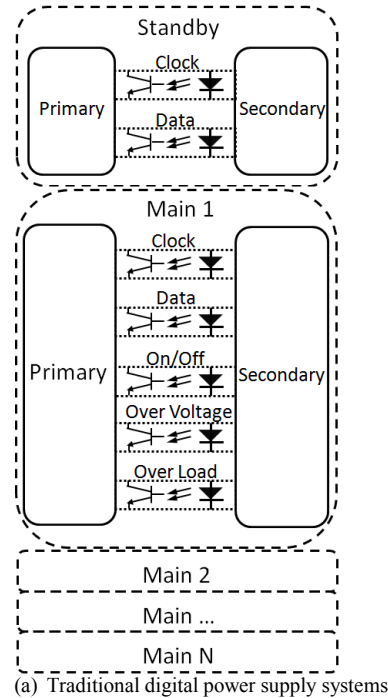

(a) The proposed digital power supply system
Fig. 1. Replacing all high-speed opto-couplers by one pulse-transformer

A pulse-transformer is the preferred isolator for the proposed system because not only it is considerably cheaper than other types of isolators, but also it can be arranged for delivering power to secondary digital circuits while transmitting data [14]. A properly designed communication protocol is required for such a system, which should be simple, minimizing the bandwidth consumption, while providing desired functions.

Many protocols developed in the past are used for digital power management rather than digital control, such as System Management Bus (SMBus), Power Management Bus (PMBus), Simple Serial Transport (SST), Universal Asynchronous Receiver/Transmitter (UART), Inter-Integrated Circuit (I^2C), Controller Area Network (CAN), Local Interconnect Network (LIN), and so on. However, most of them are designed for "event management" in large power supply systems, e.g., passing a "Failure" event from chassis to chassis, or even for a long distance [15]. These protocols are mostly in low speed, or add many framing bits into the data stream. Some studies suggest not using these protocols for transmitting real-time data [15][16][17].

Meanwhile, the isolated digital power supplies that have been developed so far use inefficient protocols for real-time communications [9][18][19], which limit the output performances, and consume more bandwidth than necessary.

In [9], a 150 MHz quad-channel isolator [20] is used to transmit duty-cycle for a 400 KHz isolated digital power supply. The duty-cycle resolution is only 400KHz/150MHz×100%=0.267%; therefore, the ADC resolution is limited to 6-bit, otherwise limit cycle oscillation will occur.

In [18], two high-speed opto-couplers are used as a data line and a clock line, respectively. The protocol used in this system transmits only 4 LSB of an 8-bit ADC. Any error value above or below this range are replaced by 1111 and 0000, respectively. The protocol extends the 4 LSB to 8 bits by doubling each bit and then adds a start sequence (0101) and a stop sequence (1010) at the beginning and the end of each frame. Every data bit is doubled, and only framing bits are singular, thus data bits can be distinguished from framing bits. The effective amount of bits transmitted in a 16-bit frame is only 4. Therefore the efficiency of this protocol is less than 25%.

In [19], UART (Universal Asynchronous Receiver/ Transmitter) standard is used in this application. The Baud Rate is configured to 2 Mbps, and each 8-bit sample is packed into a 12-bit frame, therefore its protocol efficiency is 8/12=66.7%. UART standard was not designed for real-time communications; increased software and processing effort are required to overcome problems such as clock drift, send jitter, and so on [21]. It doesn't provide features such as DC-balance to utilize cheaper isolators such as pulse-transformers, or expandable features for multiplexed use.

In this paper, an efficient communication protocol optimized for power supplies is proposed. The protocol provides functions to support the proposed architecture which replaces all isolators by a single pulse-transformer. A prototype is built to verify the effectiveness and the feasibility.

II. CONSIDERATIONS IN PROTOCOL CRITERIA

The following factors were taken into consideration when designing the proposed protocol.

1) DC-Balance

Pulse-transformer is a desired candidate of digital isolator because it is significantly cheaper than digital opto-couplers and RF-couplers.

The input signal of a pulse-transformer should be differential, and within a period of time, the amount of 1s and the amount of 0s should be equal, otherwise the pulse-transformer will be saturated by the unbalanced bit stream. Especially in power supplies, the sample data are mostly identical in steady state; therefore the pulse-transformer will be quickly saturated by the DC-imbalance. To avoid the saturation, a proper line-code must be chosen to provide DC balance within a minimum possible period of time.

2) Clock Recovery

In order to eliminate a separate isolator for the clock line, clock recovery should be used. The protocol should provide enough state change so that clock recovery is possible. The candidate line-code has to be a self-clocking code.

3) Frame Length

Variable frame length may sound a good idea because the frequency of each power stage can be different, and the output sample is ±1LSB for the most time. However, variable frame length cannot reduce the required bandwidth of the communication bus because the bandwidth must be sufficient for the worst case, where the frame needs to carry all the outputs with the maximum length.

There are benefits of using a fixed-length frame. First of all, the stop sequence can be omitted. The receiver doesn't need to know the end of the frame as long as it knows the beginning and the length. The second, for a fixed frame length the address bits can be eliminated. The samples can be organized in a certain order within a frame; therefore the address information is already contained in the order.

4) Error Detection

If a frame is found defective, it must be abandoned, but there is no need to have a mechanism to notify the secondary-side controller to send the same frame again, as the next sample is already generated. This will allow a simplified protocol to be used.

5) Control Symbols

Other than data, control symbols such as idle sequence, on/off command are also needed in the protocol. Control symbols must not be confused with sample data.

6) Time Slot

Time slot between adjacent frames is not allowed in this protocol. Because the pulse-transformer is driven by a differential input, continuous state of either logic 0 or logic 1 will quickly saturate the pulse-transformer. In order to distinguish frame from frame in the data stream, the start sequence must be distinctive from data bits.

III. THE PROPOSED PROTOCOL

A number of line codes are available. Some of the line codes are simpler and only provide solutions for one or two

criteria, such as DC-balance and/or Self-clocking. Some other line codes are more sophisticated and provide features for higher level control, such as frame synchronization and other control functions.

8B/10B Code [22] is discovered to be the most suitable line-code for the proposed protocol:

8B/10B Code only expands the original data by 1.25 times to maintain DC-balance, comparing to Manchester Code [23] which consumes twice the bandwidth.

8B/10B Code provides enough signal state transitions to support clock recovery. In the worst-case scenario, it has averagely 30 transitions per 100 digits [22].

8B/10B Code has three "comma" codes which do not occur anywhere else in a data stream by two data codes overlapping, thus they are distinguishable even when the frames lose synchronization. These "comma" codes, along with 9 other special codes, can be used as control symbols for frame synchronization, emergency shut off, and other functions.

8B/10B Code provides error detection by detecting illegal codes which violate the encoding rules. No parity bits are needed.

The mechanism of 8B/10B Code is described below: Each 8-bit code is translated into two complementary 10-bit codes. The 10B codes are selected such that they are either in the pattern of 5 0s and 5 1s, or in the pattern of 4 0s and 6 1s, or 6 0s and 4 1s. For those 10B codes that consist of 5 0s and 5 1s, their disparities are neutral. For those 10B codes that consist of 4 0s and 6 1s, and their counterpart which consist of 6 0s and 4 1s, their disparities are +2 and -2, respectively. The system's Running Disparity (RD) is monitored by the encoder: At the system's startup, the RD is 0; if the first code to send has neutral disparity, the RD stays unchanged; if the first code to send has non-neutral disparity, the encoder chooses the one that has +2 disparity, and updates the system RD to +2. If the next code sent has neutral disparity, the RD stays at +2; if it has non-neutral disparity, the encoder chooses the one that has -2 disparity to offset the system's +2 RD, and updates the system RD to 0. This way, the DC-balance is achieved within at most 6 bits.

Taking advantages of the 8B/10B Code, the proposed protocol is designed as below.

1) For single-module systems

For a single-module system the protocol is simply the 8B/10B encoding. Only 8 bits of an ADC sample can be transmitted in this protocol; this is sufficient because 8 LSBs are enough to cover the entire output regulation range. Each frame is one 10B code. In startup, a "comma" code is repeatedly sent to initialize the clock recovery and frame synchronization, and then the transmitter starts sending samples. The encoded data help clock recovery. The 8B/10B decoder detects illegal codes if the receiver receives wrong bits or loses frame synchronization.

2) For multi-module systems

Similar to the single-module mode, in multi-module mode the protocol encodes every 8-bit byte into 10 bits. However,

each frame contains several 10B codes: starting with a symbol code as a frame header, followed by a stream of data codes, depending on the number of channels. The frame header identifies the beginning of a frame, and the frame length is fixed.

In the simplest case, each frame carries samples of all channels in a fixed order: the first code following the frame header is CH1; the second code is CH2, and so on. Therefore the address bits are omitted.

In order to use the communication bandwidth efficiently when the sampling frequencies of power stages are different, several types of frames are used. The types of the frames are indicated by control symbols which are used as frame headers. No additional bits are needed. The proposed protocol requires each sampling frequency be integral times lower than the highest one in this system. For example, for a system that consists of 4 power supplies where the sampling frequencies are: CH1: 100 KHz, CH2: 50 KHz, CH3: 25 KHz, CH4: 25 KHz, the frame length only needs to be three codes instead of five. They are shown in Fig. 2.

Frame Type	Header	Byte 1	Byte 2
Type 1	Symbol 1	CH1	CH2
Type 2	Symbol 2	CH1	CH3
Type 3	Symbol 3	CH1	CH4

Fig. 2. Example Frame Types

Frame Type	Type1	Type2	Type1	Type3	Type1	Type2	Type1	Type3	…
Byte 1	CH1	CH1	CH1	CH1	CH1	CH1	CH1	CH1	…
Byte 2	CH2	CH3	CH2	CH4	CH2	CH3	CH2	CH4	…

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Fig. 3. Example Frame Sequence

Then the frame types are arranged in a sequence shown in Fig. 3 to optimize the bandwidth usage. It can be observed that CH1 takes all Byte 1 positions, CH2 takes 50% of the Byte 2 positions, and CH3 and CH4 take 25% of Byte 2 positions, respectively. When the communication bus sends 100K frames per second, all channels communicate at their own frequencies and no bandwidth is wasted, which reduces the required total bandwidth of the communication bus.

8B/10B Code provides 12 control symbols, which can be used as On/Off command, Over Voltage/Load/Temperature Protection commands, and so on; the rest of them can be used to indicate frame types. The 3 "comma" codes are recommended to be used as frame headers to regain frame synchronization in case it is lost.

IV. EXPERIMENTAL RESULTS

A prototype was built to verify the effectiveness of the proposed protocol. They system block diagram is shown in Fig. 4.
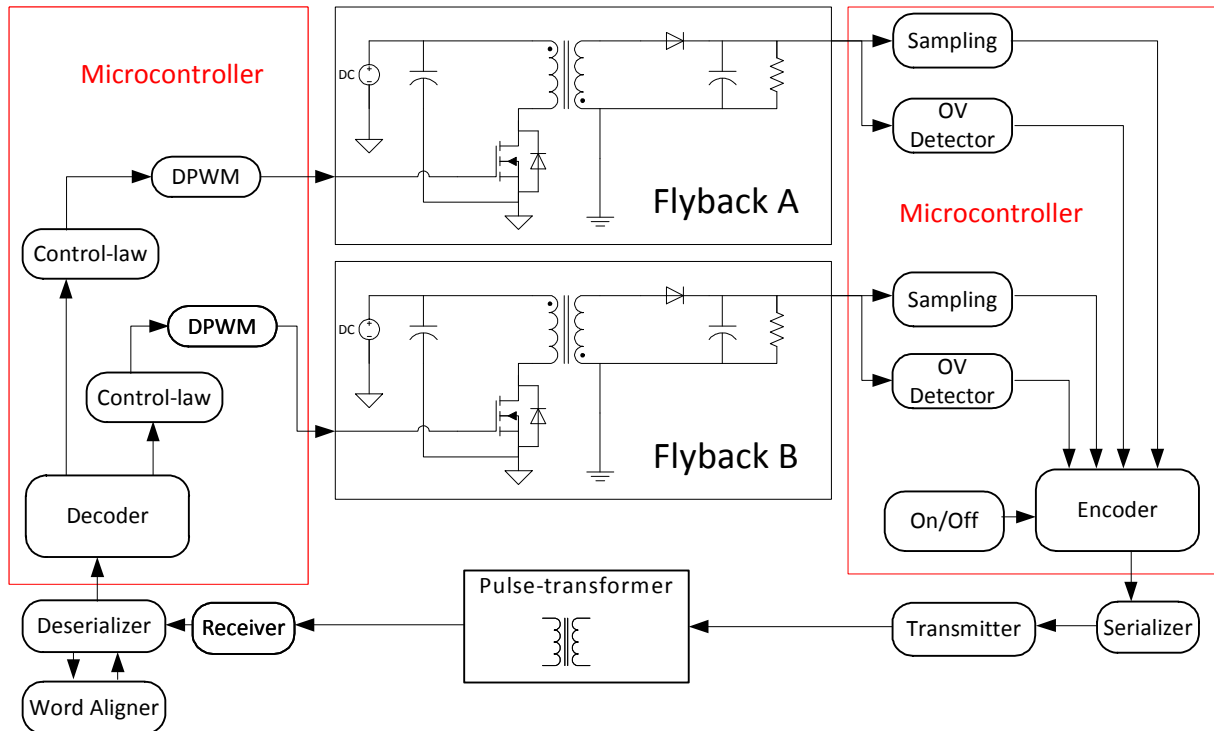
Fig. 4. System Block Diagram

The prototype consists of two identical 100 KHz digital Flyback power stages. Vin=48±5VDC, Vo=5V/25W. Two dsPIC30F2020 microcontrollers are used for implementing ADC, controller and codec. The On/Off switch and Over Voltage Protection are implemented on the secondary side, and the commands are multiplexed into the communication bus. The serializer, deserializer, and the Word Aligner are implemented by discrete ICs. The Word Aligner recognizes control symbols, and thus synchronizes the frames. A pulse-transformer is used and is driven by discrete VLDS transceivers. For simplicity, a separate clock line is used in this prototype, thus the Clock Recovery block is omitted. Nevertheless, researches [22] and many industry applications have proved that 8B/10B encoding provides good support to the Clock Recovery and the technology is mature. CPLD and FPGA manufacturers provide Clock Recovery blocks in their libraries.

Fig. 5, Fig. 6 and Fig. 7 show the output waveforms. Probe setup: Ch1 (yellow): Output voltage of Power Stage 1; Ch2 (red): Output voltage of Power Stage 2; Ch3 (blue): Output voltage of Power Stage 1, AC coupled; Ch4 (green): Output current of Power Stage 1 (Constant Resistive load).
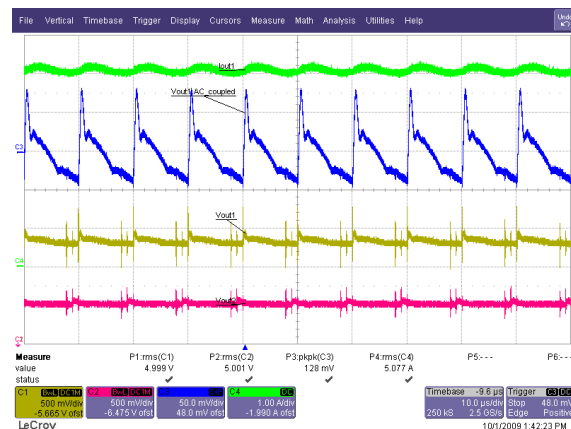

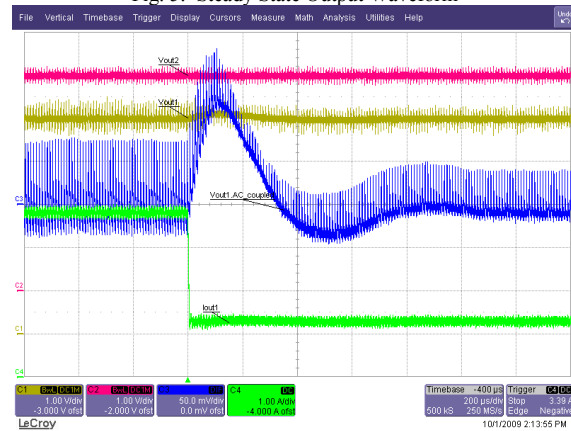Fig. 5. Steady State Output Waveform

Fig. 6. Load Transient Response 75% to 25% Load
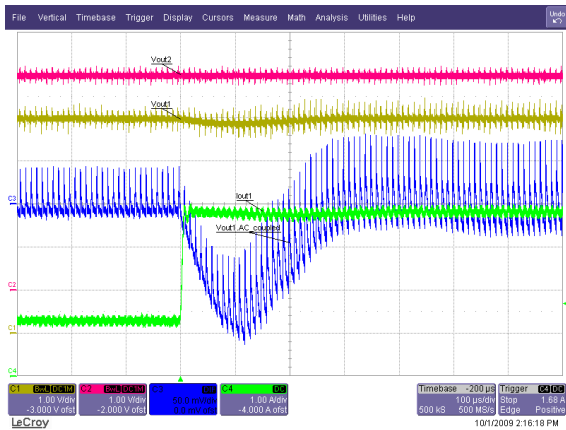
2000

Fig. 7. Load Transient Response 25% to 75% Load

Fig. 8 shows the excellent output accuracy of the prototype system.
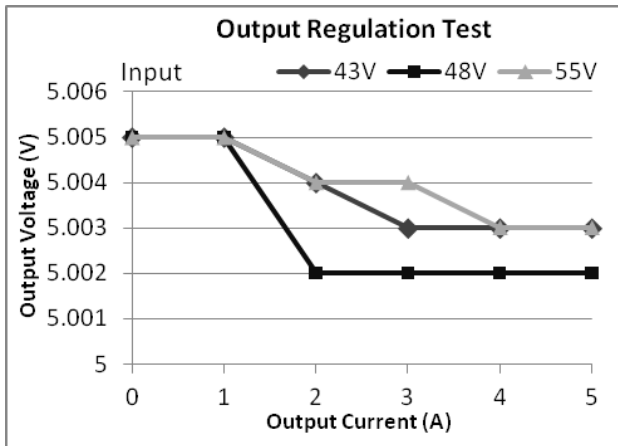

Fig. 8. Output Regulation Test

Data stream in 9 successive frames are captured in a single waveform. The waveform is then zoomed in at each frame in order to extract data that are sent from the secondary to the primary, shown in Fig. 9. Probe Setup: Ch1 (yellow): Data line; Ch2 (red): Clock line; Ch3 (blue): "Frame header received". This examines steady state operation, and also verifies the DC-balance.

The frame length used in this prototype is 8 bytes. Only the frame header and Byte 1 are used, and the other 6 bytes are left unused and are filled with "0000 0000" (corresponding to "01100 01011" in 10B code, disparity neutral). A technique is developed to use only 4 bits per sample to achieve satisfactory performance, therefore Byte 1 carries samples for both power stages (two 4-bit samples compose an 8-bit byte).
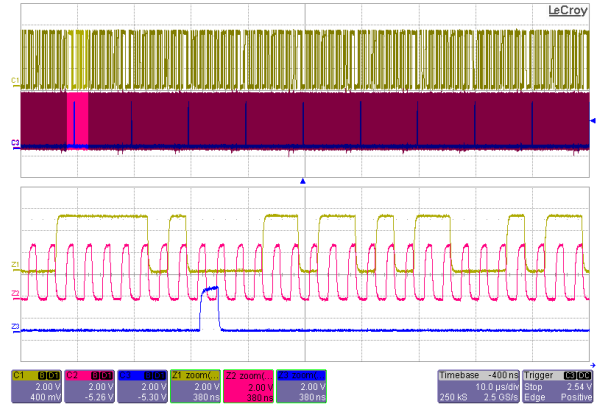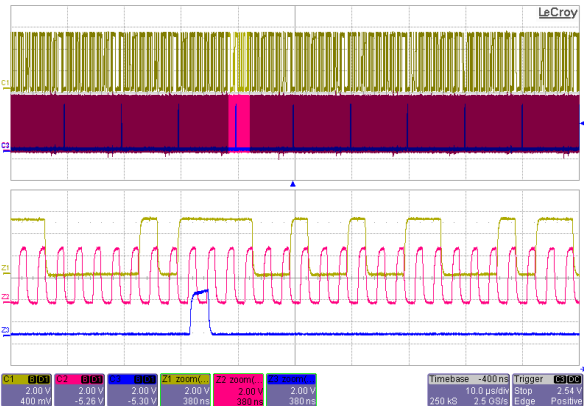
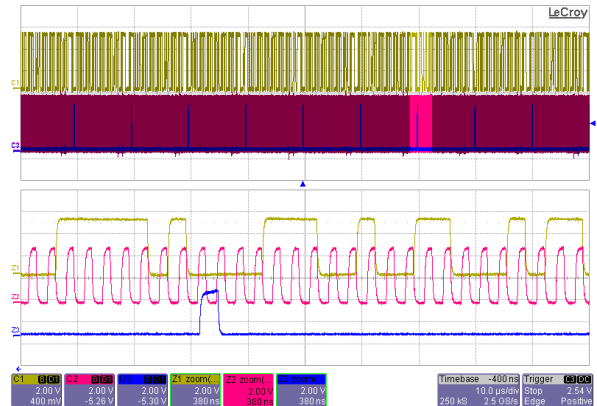
(1) Data stream (zoom-in at the 1st sample)
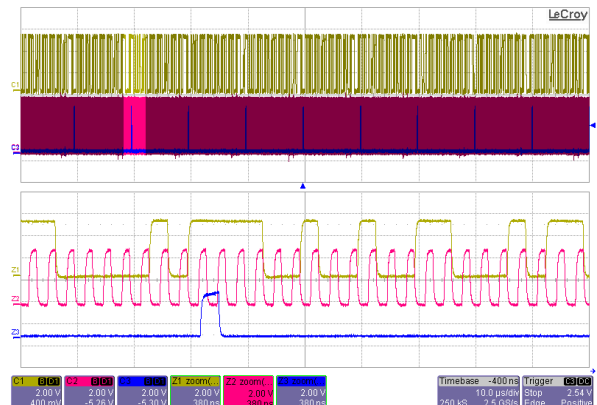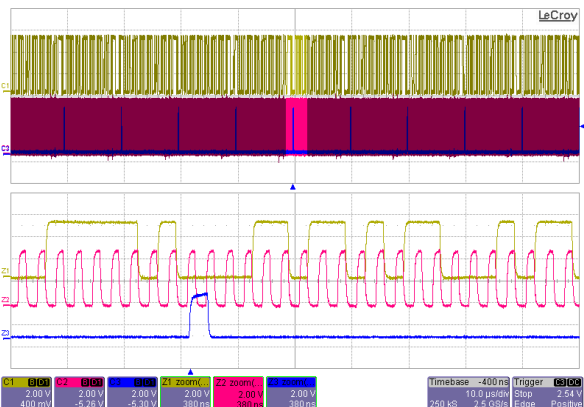

(2) Data stream (zoom-in at the 2nd sample)
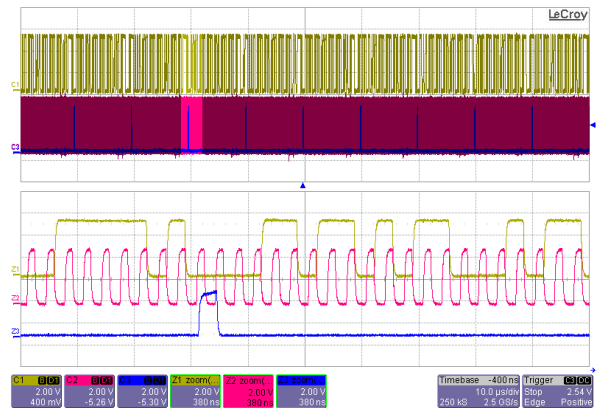
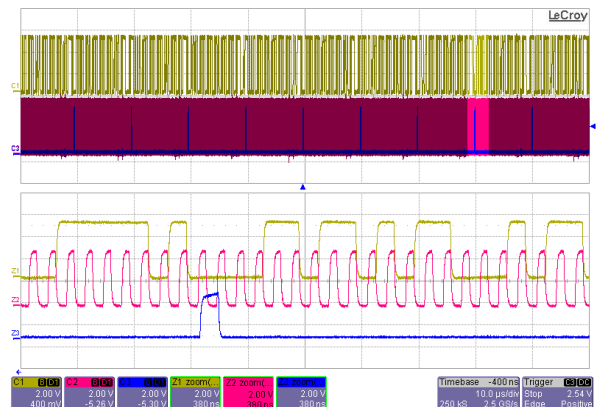(3) Data stream (zoom-in at the 3rd sample)

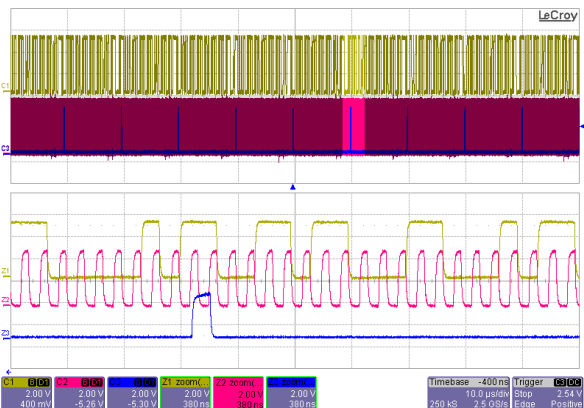(4) Data stream (zoom-in at the 4th sample)

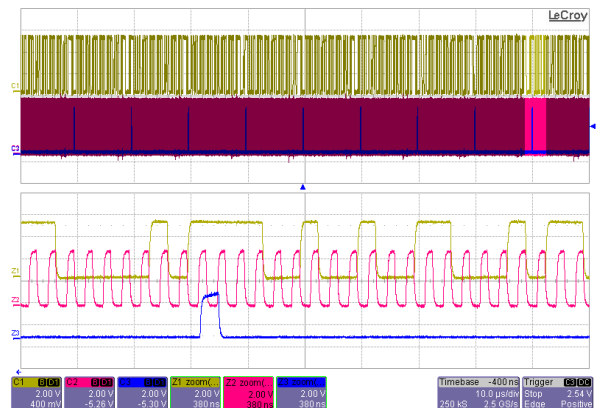
(7) Data stream (zoom-in at the 7th sample)

(5) Data stream (zoom-in at the 5th sample)

(8) Data stream (zoom-in at the 8th sample)

(6) Data stream (zoom-in at the 6th sample)

(9) Data stream (zoom-in at the 9th sample)

Fig. 9. Data stream in 9 successive frames. Ch1 (yellow): Data, Ch2 (red): Clock, Ch3 (blue): Frame Header.

The extracted data are in Table 1. The Disparity column shows that plus and minus disparity codes are chosen alternately to strictly enforce DC-balance. The 8B Code column shows that the output voltages of both power stages are regulated within 1 LSB of the reference level (1000).

Table 1 Extracted data from 9 successive frames

Frame #	Byte #	10B Code	8B Code		Disparity
			CH1	CH2	
1	header	0011111010	Comma		+2
	1	0001101101	1000	1000	0
2	header	1100000101	Comma		-2
	1	1110010010	1000	1000	0
3	header	0011111010	Comma		+2
	1	0001101101	1000	1000	0
4	header	1100000101	Comma		-2
	1	1110010010	1000	1000	0
5	header	0011111010	Comma		+2
	1	0001101101	1000	1000	0
6	header	1100000101	Comma		-2
	1	1001101100	0111	1001	0
7	header	0011111010	Comma		+2
	1	0001110010	1000	0111	-2
8	header	0011111010	Comma		+2
	1	0001101101	1000	1000	0
9	header	1100000101	Comma		-2
	1	1110010010	1000	1000	0

V. Conclusion

An efficient protocol for isolated digital power supplies is proposed in this paper. The considerations in the protocol design are analyzed. A prototype is built to prove the feasibility and the effectiveness of the proposed protocol. The protocol consumes less bandwidth than existing protocols, and significantly reduces the system cost by replacing all high-speed isolators by a single pulse-transformer.

References

[1] S. Buso, *Digital Control in Power Electronics*. Morgan & Claypool, 2006.

[2] H. Al-Atrash, "Digital Controller Design for a Practicing Power Electronics Engineer," in *Applied Power Electronics Conference, APEC 2007 - Twenty Second Annual IEEE*, 2007, pp. 34-41.

[3] S. Choudhury, "Designing the Digital Compensator For UCD91xx based Digital Power Supply," *Power Supply Design Seminar*, 2007.

[4] G. Feng, "A New Adaptive Fuzzy Logic Control Method for DC-to-DC Converter," in *Industrial Electronics Society, 2002, IECON '02*, 2002.

[5] A. G. Perry, "A Design Method for PI-like Fuzzy Logic Controllers for DC–DC Converter," *IEEE Transactions On Industrial Electronics*, vol. 54, no. 5, 2007.

[6] G. Feng, E. Meyer, and Y. F. Liu, "A Digital Two-Switching-Cycle Compensation Algorithm for Input-Voltage Transients in DC-to-DC Converters," *IEEE Transactions on Power Electronics*, vol. 24, no. 1, pp. 181-191, Jan. 2009.

[7] E. Meyer, Z. Zhang, and Y. F. Liu, "An Optimal Control Method for Buck Converters Using a Practical Capacitor Charge Balance Technique," *IEEE Transactions on Power Electronics*, vol. 23, no. 4, pp. 1802-1812, Jul. 2008.

[8] G. Feng, "A New Digital Control Algorithm to Achieve Optimal Dynamic Performance in DC-to-DC Converters," *IEEE Transactions On Power Electronics*, vol. 22, no. 4, 2007.

[9] K. Leung, "Design and implementation of a practical digital PWM controller," in *Applied Power Electronics Conference and Exposition, 2006. APEC '06. Twenty-First Annual IEEE*, 2006, p. 6.

[10] L. Balogh, "A Practical Introduction to Digital Power Supply Control," *Power Supply Design Seminar*, 2005.

[11] B. Chen, "Isolation in Digital Power Supplies Using Micro-Transformers," in *Applied Power Electronics Conference and Exposition, 2009. APEC 2009. Twenty-Fourth Annual IEEE*, 2009, pp. 2039-2042.

[12] B. Chen, "Isolated half-bridge gate driver with integrated high-side supply," in *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, 2008, pp. 3615-3618.

[13] B. Chen, "Fully integrated isolated dc-dc converter using micro-transformers," in *Applied Power Electronics Conference and Exposition, 2008. APEC 2008. Twenty-Third Annual IEEE*, 2008, pp. 335-338.

[14] R. K. Orr, Y. Liu, D. A. Brown, and R. Duvnjak, "Signal and Power Transformer Coupling Arrangements," U.S. Patent US 6,911,746 B2, Jun. 28, 2005.

[15] R. White, "Data Communications Issues For Power System Management," in *Applied Power Electronics Conference, APEC 2007 - Twenty Second Annual IEEE*, 2007, pp. 1188-1199.

[16] R. White, "Digital Power System Management," in *Proceedings Of The Applied Power Electronics Conference, APEC 2006*, 2006, pp. 176-182.

[17] R. White, "Considerations For A Power System Management Protocol," in *Darnell Digital Power Forum 2004, Presentation 5-1*, 2004.

[18] A. Prodic, D. Maksimovic, and R. W. Erickson, "Digital Controller Chip Set for Isolated DC Power Supplies," in *Applied Power Electronics Conference and Exposition, 2003. APEC '03. Eighteenth Annual IEEE*, vol. 2, 2003, pp. 9-13.

[19] "SMPS AC/DC Reference Design User's Guide," Microchip Technology Inc. DS70320B, 2008.

[20] "Quad-Channel Digital Isolator," Silicon Laboratories Si8440/1/2, 2006.

[21] W. Elmenreich and M. Delvai, "Time-triggered communication with UARTs," in *Proceedings of the 4th IEEE International Workshop on Factory Communication Systems (WFCS'02)*, Sweden, 2002.

[22] A. Widmer, "A DC-Balanced, Partitioned-Block, 8B/10B Transmission Code," vol. 27, no. 5, p. 440, 1983.

[23] W. Stallings, *Data and Computer Communications (7th ed.)*. Prentice Hall, 2004.